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Proposal for Implementation of Audio Noise Filter and Amplifier(December 2013)

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*Abstract*— This paper discuss the design and implementation of final project of EE332. This design consists of three stages: a differential stage, amplifiying stage and the buffer stage. It takes an input signal and amplifiers it with output power smaller than 1W and no distortion. Ultimately this amplifier with drive an 8 ohm speaker to play music. It generally functions to preserve the waveform and produce some gain within the power range. However, gain is limited when input is big and the power consumption is high.

*Index Terms*—Enter key words or phrases in alphabetical order, separated by commas. For a list of suggested keywords, send a blank e-mail to [keywords@ieee.org](mailto:keywords@ieee.org) or visit [http://www.ieee.org/documents/taxonomy\_v101.pdf](http://www.ieee.org/documents/taxonomy_v101.pdf" \t "_blank)

# INTRODUCTION

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he task which was assigned was to take a small signal input from a music player and amplify the signal with a loudspeaker.

## Input signal specifications

Signal voltage: 100 mVpp (min) – 5.6 Vpp (max)

Equipment available for testing:

Hardware: Oscilloscope, DMM, Signal generator

Power Supply: +/- 10 V DC

Software: Multisim

Minimum Design Specifications of the Amplifier:

Output power:1W(max)

Load Impedance (speaker): 8 Ω

Idling power: < 1W

Distortion: No audible distortion in casual listening

# Architecture and Circuit Design

The following is the diagrams of designs made of the overall circuit from datapath to transistor level.

## Block Diagram

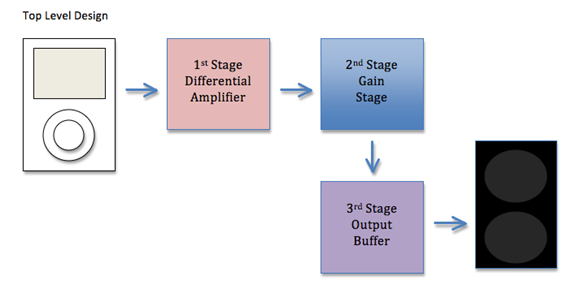


Fig I. The circuit was divided up into 3 different stages. The first stage filtered out noise. The second stage amplified the signal. The third stage provided a buffer between the load resistance and the amplification.

## Differential Amplifier

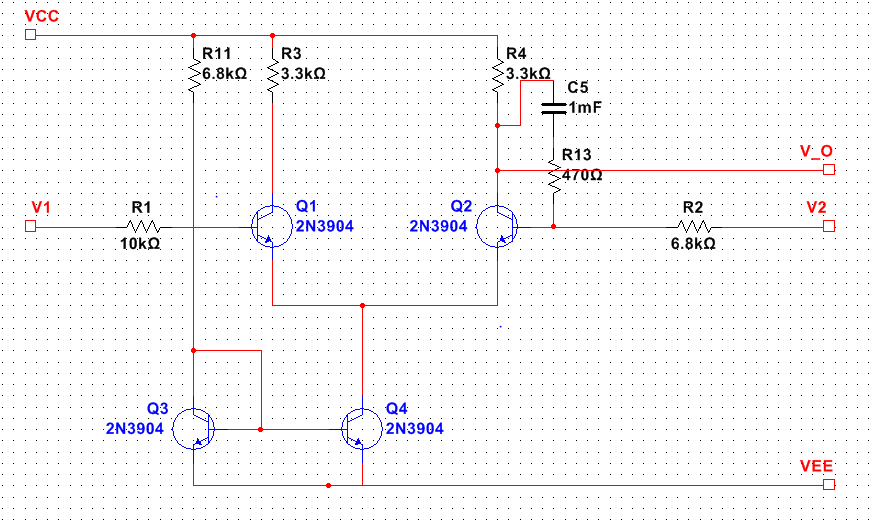


Fig II. Some notable features of the differential amplifier include the current mirror for bias and the negative feedback for stability and gain control.

## Gain Stage

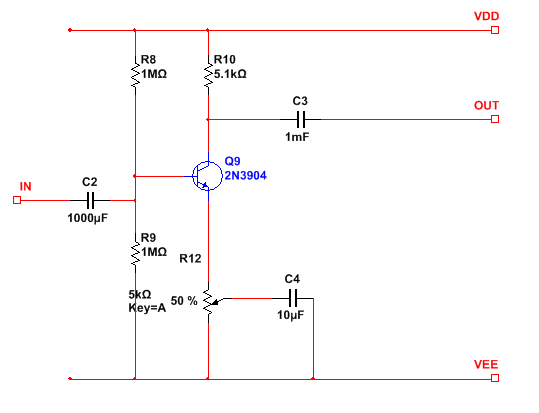


Fig III. The amplifier is a single NPN common emitter amplifier. It is AC-coupled by the two 1 mF blocking capacitors.

## Output Buffer

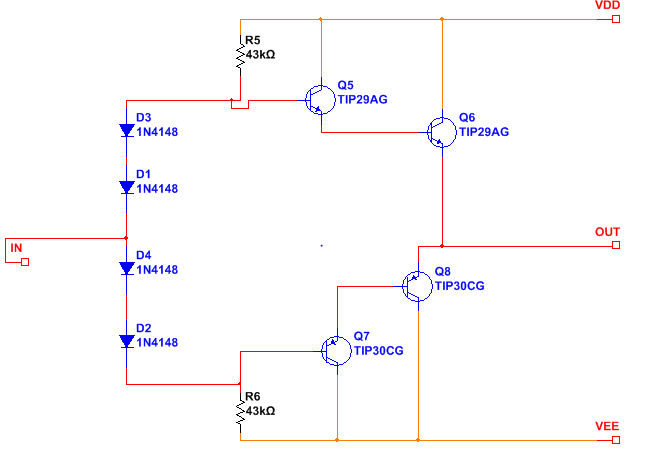


Fig IV. The output buffer is a modified AB-class output stage with a Darlington transistor configuration.

# Discussion of Circuit Topology

## Differential Amplifier Input Stage

The purpose of designing the differential input stage is to take in an AC voltage input and convert it into an output current that heads into the second stage. The resultant output voltage is the difference between the two signals. The differential stage is used to filter out noise from the ground. This was very critical since we were using unshielded breadboards.

Since the design topology of an amplifier can be found in many examples already built, we first started with using an NPN transistor in our design. Since there is only one signal input, V2 is grouded and the V1 is connected to function generator. The output is the collector the NPN Q2. Standard current mirror setup is installed at the emitter to stablize the operational points and increase REE, since the Q-point is directly dependent on negative power supply and emitter resistance limits the CMRR.

The differential amplifier was biased using a current mirror instead of a resistor. This allowed us to have more control over the Q-point of our output, which allowed for more swing. For the convenience of assembling and saving space, we use a CA3046 NPN array with differential pair embedded to construct the first stage. Also two transistors inside serve as the current mirror.

We have a negative feedback loop from the inverted input of the differential amplifier to the output. This gave us stability the output and further control of gain in our differential amplifier.

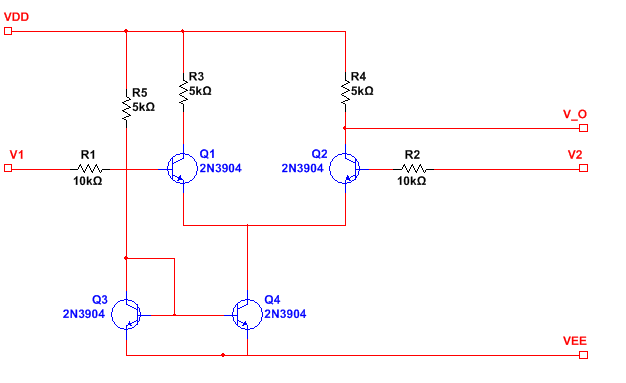


Fig I.

The Q-point analysis

Assume Q3 and Q4 are forward biased,

 (1)

The single ended gain is gmRc/2 is approximately is 93, which is not reasonable.

Later we found that the collector current is a little bit small and the collector voltage is higher than expected, since clipping occurs when input increases to So a feedback loop from the v2 to output terminal to stablize both the collector current and lower the potential of output terminal.

The following is the testing result when the input is CH1 and the output is CH2 for differential stage.

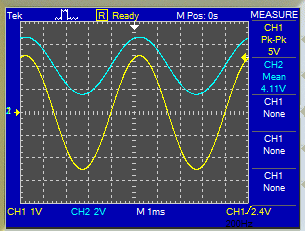


Fig V. The gain of the differential amplifier is approximately 1.

## Common Emitter Amplifying Gain Stage

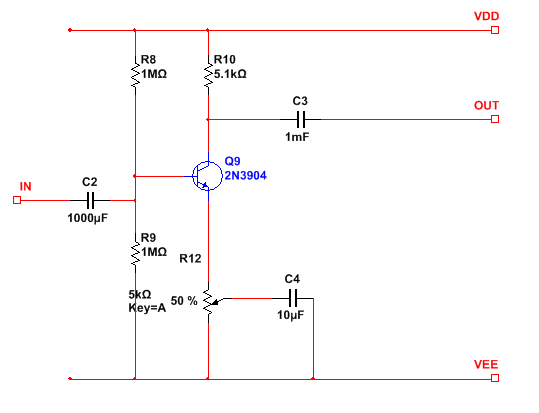


Fig. II.

In the gain stage, also called trans-impedance stage, the current from stage one flows in and is converted into voltage. This is where most of the gain occurs and is then pushed to the output buffer stage. In between each stage transition, we decided to place a capacitor to block the DC component from entering into the next stage.

The basic topology of building a gain stage was first found in the lab reports we previously did during the quarter. Our design then began to evolve as we researched other topologies for designing the second stage. In the first itineration of the stage, we use the common-emitter setup to amplify the signal. A single transistor common emitter stage allowed for adjustable gain within the range that we needed, while being simple and easy to connect.

We used blocking capacitors to AC couple the gain stage from the other stages. While this made low frequencies suffer gain loss, this allowed us to have easier control over the DC biases of all the transistors.

Multisim simulation measures the operating points under DC bias as follows

|  |  |
| --- | --- |
| collector current Ic | 1.11mA |
| base voltage | -3.76V |
| collector voltage | 4.35V |
| emitter voltage | -4.42V |

So the Q-point is (1.11mA, 8.77V), and the base-emitter voltage is about 0.65V, which means transistor is in forward active region.

As for the common emitter, the terminal gain is given by

 (2)

which is approximately the load resistance over emitter resistance. In this setup the load is the parallel of collector resistance and the input resistance of final stage. Simulation shows that the common emitter operates at the appropriate bias and provides reasonable gain.

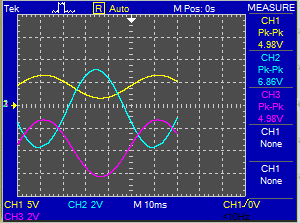


Fig. VI. High input with gain 1.3

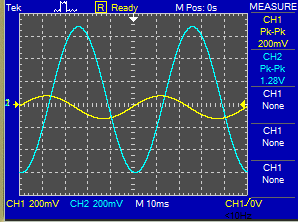


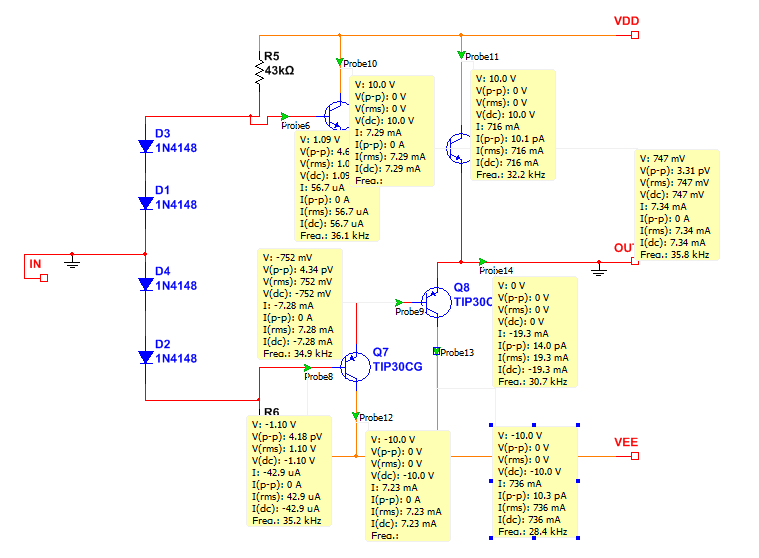
Fig. VII. Gain approx. 6 at input Vpp = 0.2V

In the design, we include a potentiometer to adjust the ratio of emitter resistance and better control the gain.

## Class-AB Emitter Follower Output Buffer Stage

We decided to use a class AB configuration for our output stage, because of its power efficiency and its linearity. We used a Darlington emitter follower configuration for the transistors because it does not amplify voltages, having a gain of one, while also having a high input resistance. This allows more voltage to be “seen” by the buffer.

In using the Darlington set-up, one drawback was that we were doubling the base-emitter voltage. The current flowing through was too high and so to combat that we doubled the number of diodes used in the set-up and increased the value of the resistors connected in parallel.

Fig. IX. This shows the buffer stage with Q-points calculated.

|  |  |
| --- | --- |
| Q points |  |
| Q5 | 7.29mA, 9.3V |
| Q6 | 716mA, 10.2V |
| Q7 | 7.23mA, 9.3v |
| Q8 | 736mA, 10.2V |

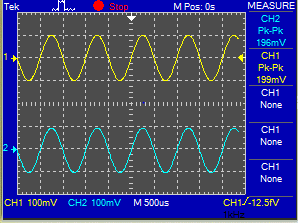


Fig. X. The buffer is tested at low voltages.

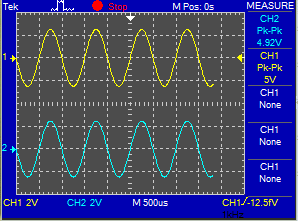


Fig. XI. The buffer is tested at high voltages.

# Assembly and Testing

But when we transferred our initial values for resistors which we calculated to simulation, we found that many of the gains were off. In particular, while we calculated a gain of 96 in the differential amplifier, we actually ended up with a gain of less than one. This was caused by the resistor in the V1 input causing a voltage drop, so that the input actually “seen” by the differential amplifier was less than we expected. This was not considered in our calculation. This, the desire for higher output swing, and some reliable form of volume control was our motivation for including a gain stage.

Our initial design for the differential amplifier did not include a feedback loop. This caused strange effects including our output DC voltage to be very close to rail, when it worked fine in simulation. By including the feedback loop that we did, we were able to stabilize our differential amplifier.

We tested the circuit in simulation extensively to fine tune our resistor values. The 43k resistor in the buffer and the various gain stage resistances were all obtained using PSPICE.

# Circuit Performance

|  |  |
| --- | --- |
| max output power(Vpp) | 5.67V |
| 0.5 frequency range(Vpp) | 0.05V |
| Idling power | 20V\*0.07A = 1.4W |

## Input resistance

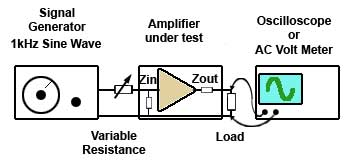


Fig. XII. The circuit used to test input resistance.

We tested the input resistance using a potentiometer and a 330k resistor. The idea is that connect the testing resistor in series with the input of audio amplifier. Adjust the potentiometer and let the voltage of amplifier exactly the half of testing input. Measure the testing resistor and the input resistance should be equal to this value.

The input resistance of our amplifier is 430kΩ, and it satisfies the general principle that input resistance should be high to preserve the input signal.

## Output resistance

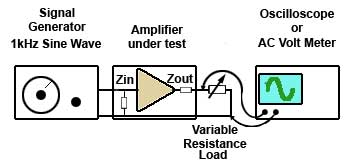


Fig XIII. The circuit used to test output resistance.

First connect the output to no load, measure the voltage V1. Then connect the output to a potentiometer with maximum resistance of 20Ω. Turn on the amplifier and gradually decrease the potentiometer until the output voltage is roughly half of V1. Measure the potentiometer and the value is the output resistance.

Our output resistance is 0.8Ω, which satisfies the general principle of small output resistance.

# Conclusion

Lots of hours have been used in order to meet the guideline of the design project. Numerous attempts on the project lead us to get a completed audio amplifier as the specifications and requirements. It generally serves as an amplifier with adjustable gain. It was tested during demonstration where it received a audio input from computer and outputted the music to a speaker. When we adjusted the emitter resistance of common-emitter amplifier, the volume, which is the magnitude of output signal, was changing accordingly.

However there are some drawbacks. The biggest one is the limited gain. During demonstration, the output was really small, even going below the input. We later checked the circuits, and it was because the extra resistance that we would like to remove was connected to the amplifier output. But bigger issue also is concerned with the circuit design. This amplifier works great at low input, but the gain is small if input is high. This is probably because the bias doesn’t allow maximum swing. Also there is a trade-off between the output power and the gain. If connecting resistance to lower the output power, this will decrease the gain as well. So a better solution will be to control the power consumption and does not influence gain.

The output stage could be improved further, since some two transistors are not in forward active region. Although separately tested well, if the input of the final stage has a DC shift, the output will likely be distorted. Something could be done with the Darlington structure or a standard class AB may buffer the signal better

Overall the design functions as an amplifier, but further designs should be optimized to provide bigger gain and limit the power consumption.

# Parts Cost

|  |  |  |
| --- | --- | --- |
| **BJT** | **Model** | **Cost** |
| **Q5, Q6** | **TIP29AG** | **.20 (x2)** |
| **Q7, Q8** | **TIP30CG** | **.20 (x2)** |
| **Q1, Q2, Q3, Q4** | **CA3046** | **1.95(x1)** |
| **Diode** | **Model** |  |
| **D1, D2, D3, D4** | **1N4148** | **.15 (x4)** |
| **Resistor** | **Model** |  |
| **R1** | **10 kΩ** | **.10** |
| **R2, R11** | **6.8 kΩ** | **.10(x2)** |
| **R3, R4** | **3.3 kΩ** | **.10(x2)** |
| **R5, R6** | **43 kΩ** | **.10(x2)** |
| **R7** | **8 Ω** | **.10** |
| **R8, R9** | **1 MΩ** | **.10(x2)** |
| **R12 (potentiometer)** | **5 kΩ** | **.10** |
| **R13** | **470 Ω** | **.10** |
| **Capacitor** | **Model** |  |
| **C2, C3, C5** | **1 mF** | **.25 (x3)** |
| **C4** | **10 uF** | **.25** |
|  | **Total =** | **$7.50** |

References

*Basic format for books:*

1. Richard C. Jaeger and Travis N. Blalock, *Microelectronic Circuit Design, 4*th ed. New York

1. This paper is was submitted on December 8, 2013. Financial considerations were provided by our wallets.

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